FLIP CHIP IN LEADED MOLDED PACKAGE WITH TWO DIES

BACKGROUND OF THE INVENTION

1. Field Of the Invention

The present invention relates to a flip chip in a leaded molded package, and more particularly, to a flip chip in a leaded molded package with two stacked dies.

2. Description Of The Prior Art

Semiconductor devices are becoming smaller and smaller. Additionally, as the need for speed, power and capacity increases, such a reduction in size leads to a contradiction in that smaller devices often have smaller capabilities.

In order to create smaller devices but with increased capabilities, the prior art has attempted to stack dies on top of one another. However, the prior art currently uses wire bonding for its interconnect scheme, which leads to higher resistance and inductance and does not allow for as thin a package as desired. Additionally, using wire bond techniques does not allow for the drain regions of a power MOSFET die to be exposed.

SUMMARY OF THE INVENTION

The present invention provides a chip device that includes a leadframe or a substrate that includes a plurality of leads. A first die is flipped onto the leadframe and the leadframe and die are then flipped together. A second die is then flipped onto the leadframe. The two dies are coupled to the leadframe with solder bumps. A molded body is placed around the dies and the leadframe such that the drain area of at least the first die is exposed.

In accordance with one aspect of the present invention, the first die is attached to the leadframe with a higher temperature reflow process while the second die is attached to the leadframe using a lower temperature reflow process.

In accordance with another aspect of the present invention, the first die of the chip device is a MOSFET while the second die is a controller IC.

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PATENT APPLICATION

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Thus, the present invention provides a chip device that includes two dies stacked atop one another. The use of solder bumps allows for a small profile package. In addition, the non-use of wire bond interconnect allows for accommodating a very large size die for a given molded package body outline. A die size in excess of 150% of the nominal wire bonded package size may be accommodated by this arrangement.

Other features and advantages of the present invention will be understood upon reading and understanding the detailed description of the preferred exemplary embodiments, found hereinbelow in conjunction with reference to the drawings in which like numerals represent like elements.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a side sectional view of a chip device in accordance with the present invention; and

Figure 1A is a schematic side sectional view of a bumped die.

DETAILED DESCRIPTION OF THE PREFERRED EXEMPLARY EMBODIMENTS

Figure 1 provides a cross-sectional view of a chip device 10 with a leaded molded package in accordance with the present invention. The device includes a leadframe 11, two dies 12, 13 coupled to the leadframe and a molded body 14 placed around the coupled dies and leadframe. The leadframe includes a plurality of leads 15.

The chip device is preferably created by placing the leadframe "upside-down" and flipping first die 12 onto the backside of the leadframe. Preferably, the die is what is commonly referred to in the industry as a "bumped die." Alternatively, solder paste or solder bumps may be placed onto the leadframe prior to flipping the die thereon. The die is then attached to the leadframe with a high temperature reflow process.

First die 12 is preferably a one-piece item that is often referred to in the art as a "bumped die." As can be seen in Figure 1A, a bumped die includes first die 12, "under bump material" that serves as an intermediate layer 26 between the top surface of the die and solder bump 22, and the solder bumps themselves. Preferably, the under bump material is one of TiW, Cu, Au or an equivalent. In the example illustrated in Figure 1A, the under bump material is broken into three layers – Cu plating 26a, sputtered Cu 26b and sputtered Ti 26d.

The leadframe with the first die coupled thereto is then flipped. Second die 13 is then attached to the top side of the leadframe. Once again, the second die is

preferably a bumped die. Alternatively, solder bumps or solder paste may be placed onto the leadframe prior to placing the die thereon. In order to avoid the first die solder from reflowing, a lower temperature reflow process is used to reflow the solder between the second die and the leadframe. The "higher" temperature solder preferably has a melting around point 310°C, and could be for example, 95/5 Pb/Sn. The "lower" temperature solder Sn/Sb having a melting point around are 250°C.

Molded body 14 is then placed around the leadframe and the dies coupled thereto. Preferably, drain region 20 of the first die is exposed through the body. Additionally, back side of the second die may be exposed through the top of the body where an optional heat sink may be attached for further improved heat dissipation.

Thus, the manufacturing process may be used to produce high density packaging, when a higher cell density silicon is not available, or when the higher cell density silicon die size is so large that it will not fit into a small package. In memory devices, a mirror image of two identical dies being stacked together creates a higher density memory cell with a smaller footprint. In intelligent load switches (ILS), a higher pin IC may be effectively combined with a three-terminal MOSFET to produce a package with the smallest number of pins (smallest package) as the drain region of the MOSFET may be connected to the printed circuit board (PCB) directly due to the draining region being exposed through the bottom of the body, thus, directly saving I/O pins on the package. A high current intelligent load switch may therefore be constructed that has the dual advantage of small footprint and very superior thermal performance.

Additionally, the present invention may be used to create a chip device arrangement where a controller IC is combined with a MOSFET in a small package outline, thus forming the intelligent load switch. Since the backside (drain) region of first die 12, the MOSFET, is exposed, it may be attached directly to the PCB to provide a good thermal path and a low resistance drain contact. The arrangement saves a couple of I/O pins that allows the package to have a low I/O count, thus reducing its size. Connections between the IC's and the MOSFET's source and gate may be accomplished easily by routing the leadframe as needed, facilitating a low-resistance (high current) connection.

The use of solder bumps in the chip device also contributes to the small profile package (either through use of solder bumps directly or through use of a bumped die), e.g., each die may be 8 mils thick, the solder bumps may be 6 mils, the leadframe about 6 mils, and the molded body about 6 mils, thus giving a total package height of

approximately 34 mils (0.8 mm). In addition, the non-use of wire bond interconnect allows for accommodating a very large size die for a given molded package.

Although the invention has been described with reference to specific exemplary embodiments, it will appreciated that it is intended to cover all modifications and equivalents within the scope of the appended claims.